Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claim 40, and add new claims 44-53 as follows:

Listing of Claims:

1-39. (Canceled)

40. (Currently Amended) A method for executing read and write commands in a memory system having a bidirectional memory bus coupling a controller to a first, second, and third memory hub, the second memory hub being downstream from the first memory hub, and the third memory hub being downstream from the second memory hub, the method comprising:

the controller issuing a read command to access a first memory location in a first memory device coupled to the second memory hub; ~~in the memory system;~~

after the controller issues the read command and before receiving the read data, ~~before completion of the read command, scheduling~~ the controller issuing a write command to write data to a second memory location in a second memory device coupled to the third memory hub, the controller further providing write data corresponding to the issued write command to the bi-directional memory bus; ~~in the memory system;~~

retrieving read data corresponding to the issued read command from the first memory location and providing the read data to the bi-directional memory bus;

~~prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;~~

the controller providing a bypass enable signal to the first memory hub;

~~in the memory system, bypassing~~ in response to receiving the bypass enable signal, the first memory hub storing the write data to allow the read data on the bidirectional memory bus to be coupled to the controller; and

~~receiving the read data on the bidirectional memory bus from the memory system; and~~

the first memory hub providing the write data to the bidirectional memory bus.

41. (Original) The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. (Original) The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. (Original) The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

44. (New) A method for writing data to a memory location in a memory system, the memory system including a controller coupled to a first, second, and third memory hub by a bidirectional memory bus, the second memory hub being located downstream from the first memory hub, the third memory hub being located downstream from the second memory hub, the method comprising:

the controller issuing a read command to a first memory location of a first memory device coupled to the second memory hub;

after issuing the read command, issuing a write command to a second memory location of a second memory device coupled to the third memory hub and providing write data corresponding to the issued write command to the bidirectional memory bus;

coupling the read data corresponding to the previously issued read command to the bidirectional memory bus;

the controller or a memory hub providing a bypass enable signal to the first memory hub;

in response to the bypass enable signal, coupling the write data to a register in the memory system for temporary storage of the write data to allow the read data corresponding to the previously issued read command to propagate on the bidirectional data bus;

recoupling the write data stored in the register to the bidirectional memory bus; and

writing the write data to the memory location.

45. (New) The method of claim 44 wherein issuing the read command to the memory system precedes issuing the write command to the memory system.

46. (New) The method of claim 44 further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

47. (New) The method of claim 44 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

48. (New) A method for executing memory commands in a memory system having a bidirectional memory bus on which both read and write data can be coupled, the memory system including a controller coupled to a first, second, and third memory hub, the second memory hub being downstream from the first memory hub, the third memory hub being downstream from the second memory hub, the method comprising:

the controller issuing a read command to a first memory location in a first memory device coupled to the second memory hub;

the controller issuing a write command to a second memory location in a second memory device coupled to the third memory hub and providing write data corresponding to the write command to the bidirectional memory bus of the memory system after issuing the read command;

accessing read data from the first memory location, the read data corresponding to the previously issued read command;

coupling the read data corresponding to the previously issued read command to the bidirectional memory bus;

the controller or a memory hub providing a bypass enable signal to the first memory hub;

in response to the bypass enable signal, decoupling the write data in the first memory hub from the bidirectional memory bus preventing a collision between the read data and the write data;

propogating the read data on the bidirectional memory bus through the first memory hub; and

recoupling the write data to the bidirectional memory bus.

49. (New) The method of claim 48 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

50. (New) The method of claim 49 further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

51. (New) The method of claim 49 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

52. (New) A memory system comprising:

a controller configured to issue read and write commands and to issue write data to a bidirectional memory bus, the controller further configured to issue a bypass enable signal;

a first memory hub coupled to the controller by the bidirectional memory bus, the first memory hub including a bypass circuit configured to receive write data from the

bidirectional memory bus and store the write data in response to receiving the bypass enable signal from the controller; and

a second memory hub coupled to the first memory hub and the controller by the bidirectional memory bus, the second memory hub coupled to at least one memory device and located downstream from the first memory hub, the second memory hub configured to provide read data to the bidirectional memory bus, wherein the bypass circuit in the first memory hub is configured to store the write data in response to receiving the bypass enable signal to allow the read data to propagate on the bidirectional memory bus through the first memory hub and prevent a data collision between read data and write data on the bidirectional memory bus.

53. (New) The memory system of claim 52 wherein the bypass circuit comprises a register configured to receive and store the write data.